C2OI

High-Efficiency 'Receiverless' Optical Interconnects

DARPA

Objective

Develop novel, high-efficiency, high-power, and high-speed transmitter and receiver modules to minimize additional support electronics in chip-to-chip optical interconnects

Unique features

- **Transmitter:** Small footprint integrated laser-modulator; high-κ grating; 45-degree facet for vertical; backside microlenses; quantum-well intermixing(QWI) for multiple-bandgaps
- **Receiver:** Digital receiver architecture; high-saturation power PDA photodetector design; crosstalk shielding

Approach

- Design & simulate transmitter and reciever modules
- Refine new technologies such as QWI, 45-degree facets, microlenses, air-bridge contacts, and shielding
- Fabricate & test device arrays
- Provide samples to industrial collaborators.
- Re-spin designs to respond to system's needs; fabricate & deliver new modules

Milestones—Phase I

• Design and simulate to verify power budget and other aspects	6 mo.
• Demo high-efficiency, high-power laser-mod and photodetectors	15 mo.
• Demo module arrays and deliver samples	18 mo.

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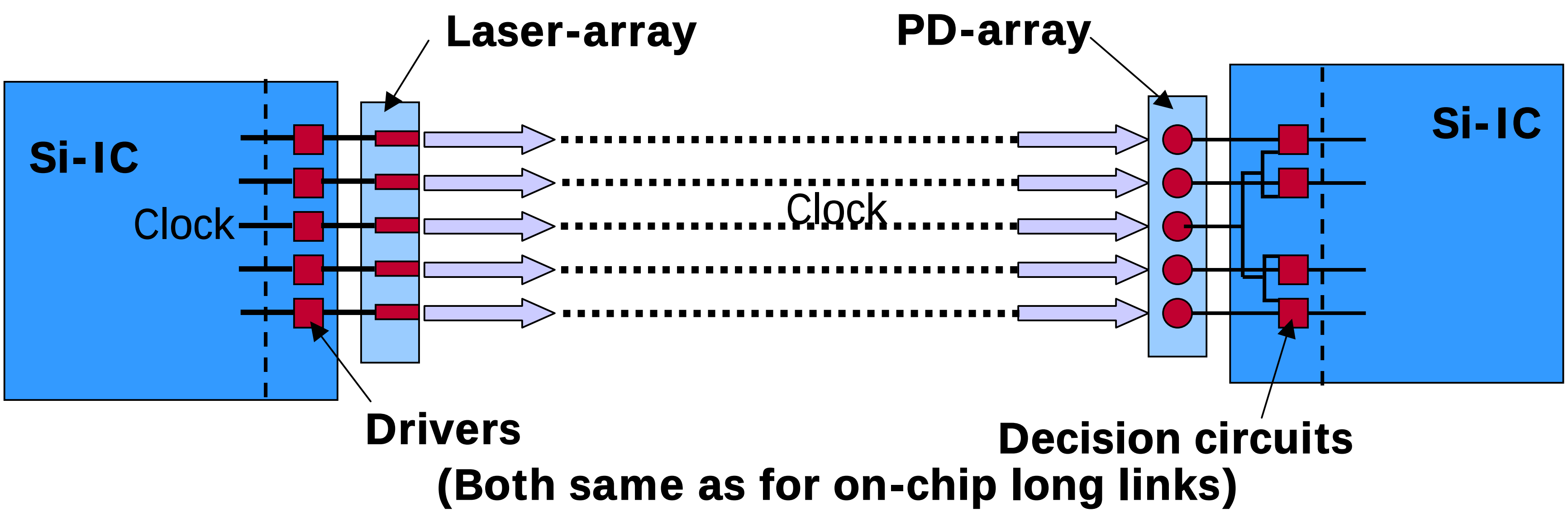
Interconnect architecture



Criteria/Concepts

Criteria

- Support data rates up to 40 Gbs
- Small footprint and low power dissipation

Concepts

- Avoid additional driver/receiver electronics
- Use integrated in-plane laser-modulator at ~ 980 nm to get bandwidth and power required at high efficiency
- Use high saturation power photodetector to directly drive logic (or same Si receiver as used for electrical interconnects)

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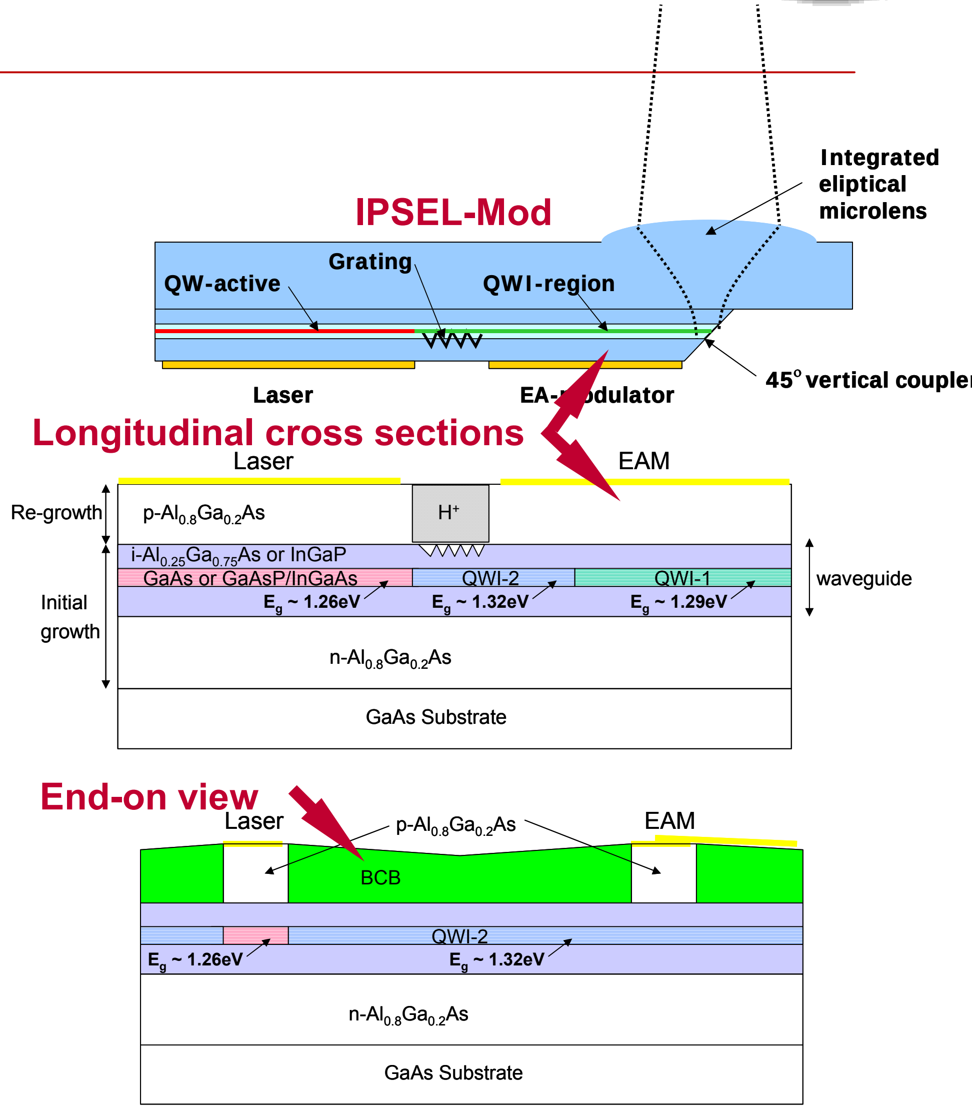
Technical Approach: Transmitter

- Single-regrowth, small-footprint integrated DBR-laser--EA-modulator design
- High-κ grating to minimize footprint and loss
- 45-degree facet for vertical emission and no reflections
- Backside microlenses
- Quantum-well intermixing(QWI) for multiple-bandgaps to simultaneously optimize laser, grating, and modulator sections



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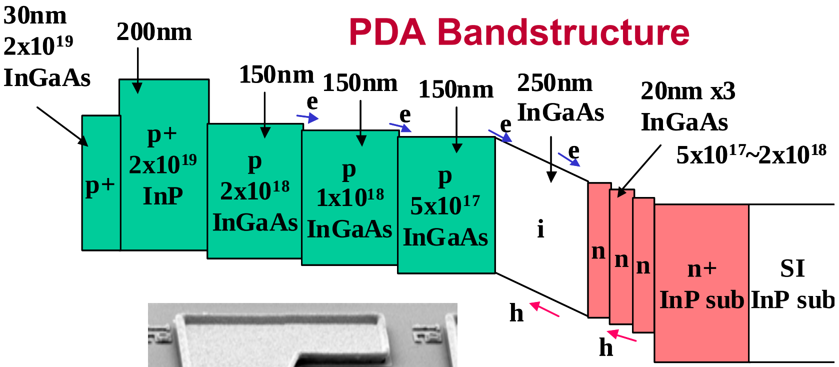
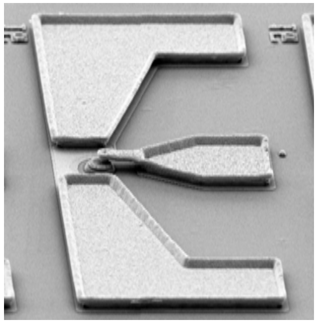
Technical Approach: Receiver

- Digital receiver architecture to eliminate receiver electronics and associated latency, noise and dissipated power
- High-saturation-power PDA photodetector design to deliver high currents at high bandwidths
- Air-bridge contacts for low stray capacitance
- Crosstalk shielding to eliminate effect of stray light

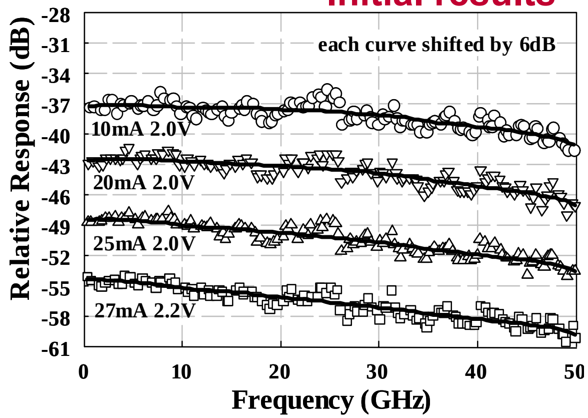
PDA Bandstructure





Air-bridge contacts

Initial results



Past Work: transmitters

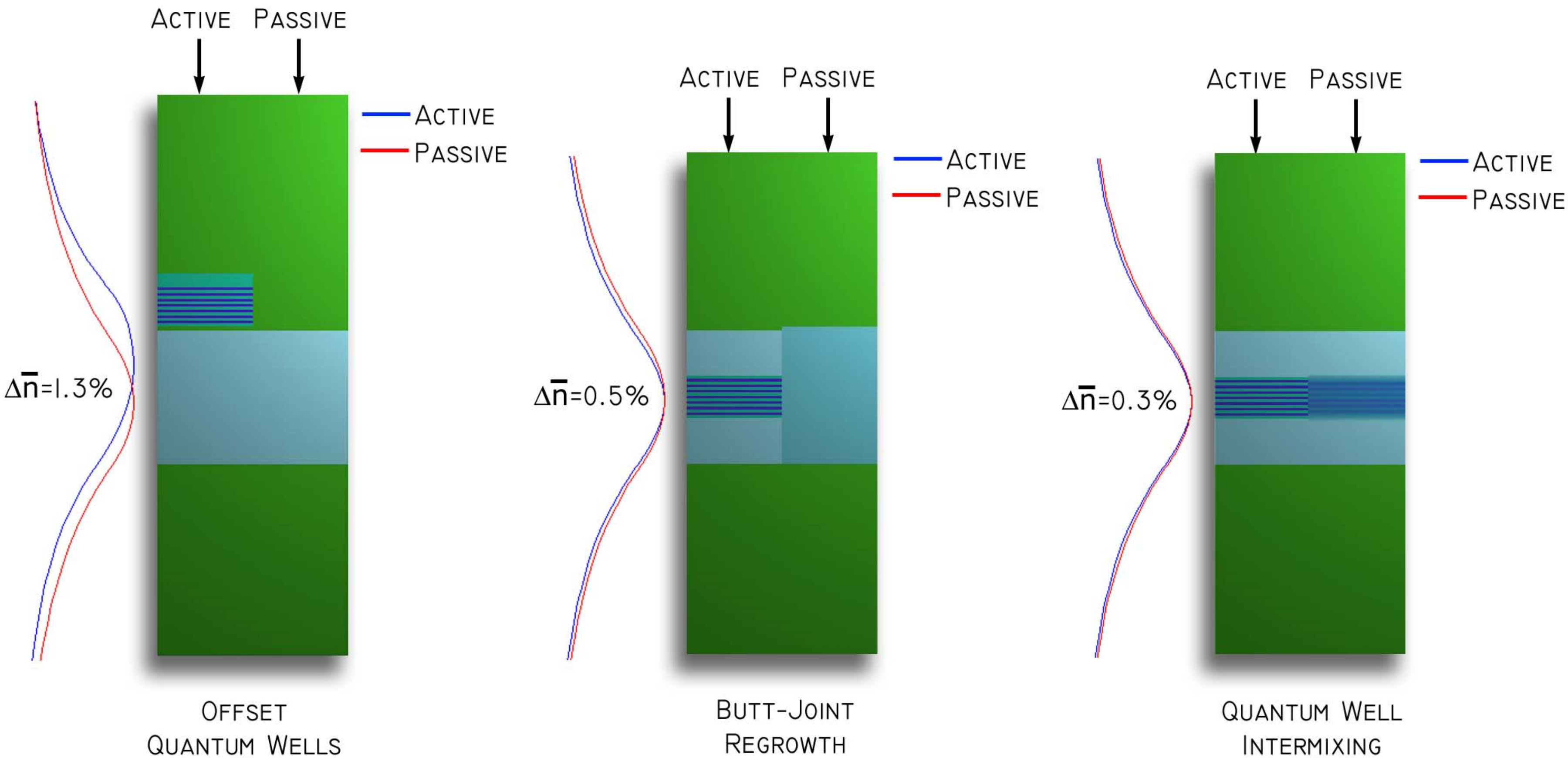
Active-Passive Integration

Modulators

Quantum-well intermixing

VCSELs/Microlenses

Active-passive integration



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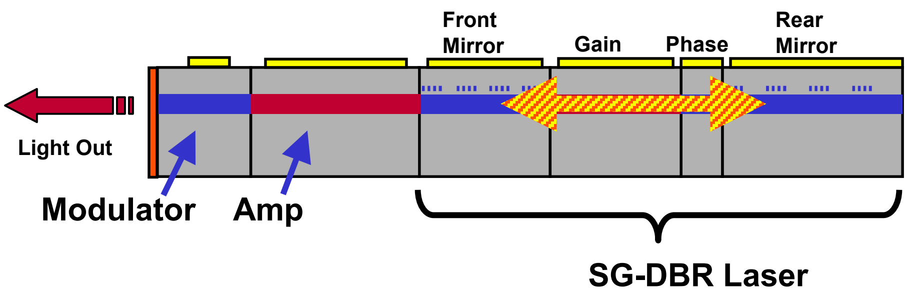
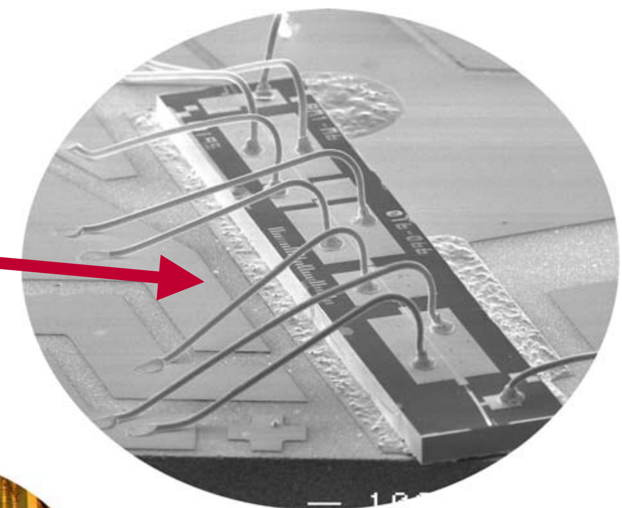
Commerical SGDBR-SOA-EAM

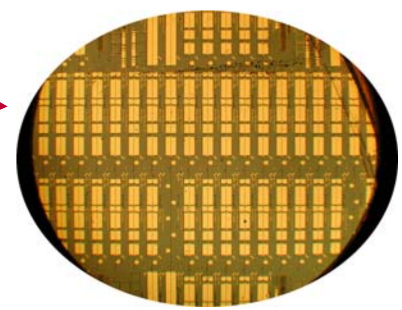
- Single-chip integrated tunable laser and modulator
- Common waveguide throughout





6 section InP chip

- On Wafer Testing



✓ High yield
  - Will be more like semiconductor ylds

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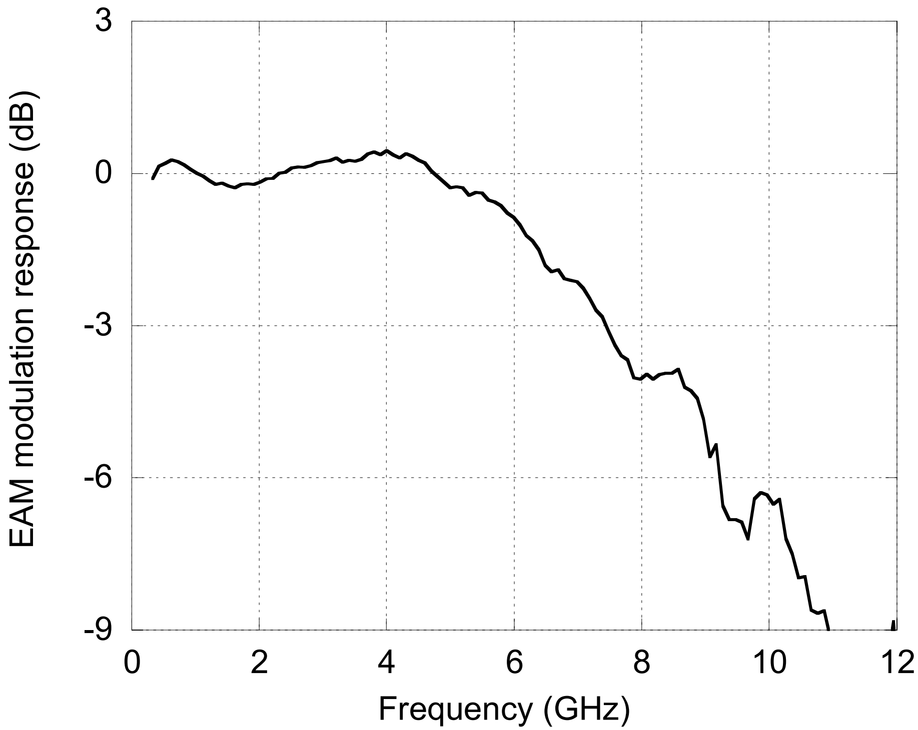
Lumped EAM modulator performance



➢Typical bandwidth measurement for a lumped 250μm long device

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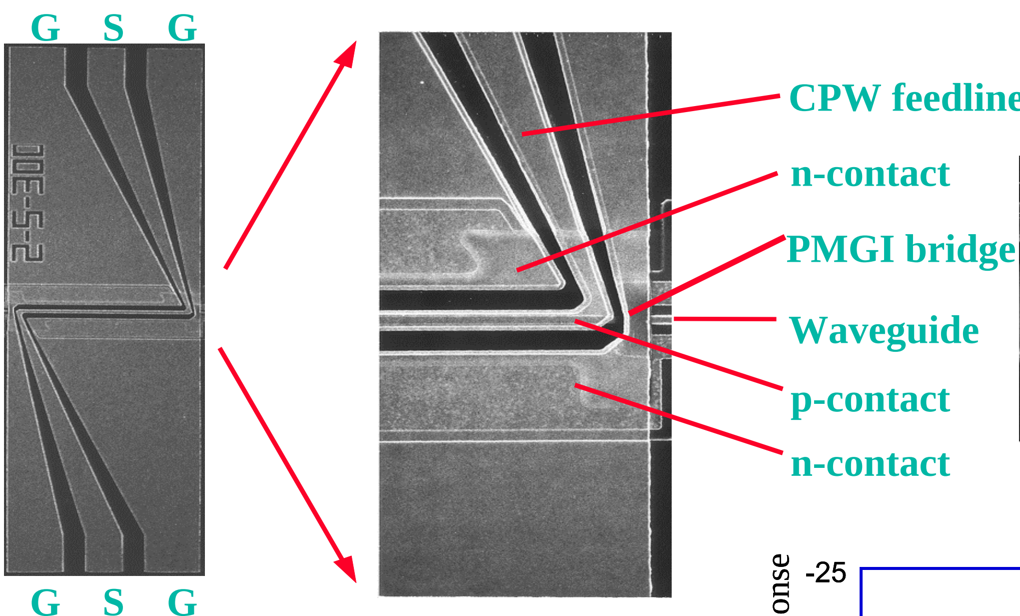
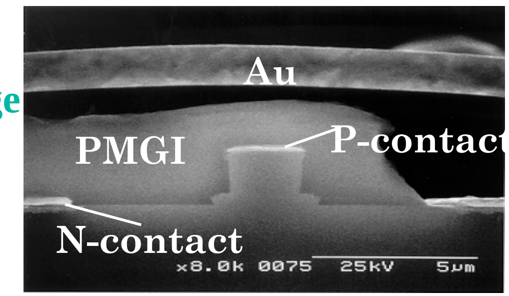
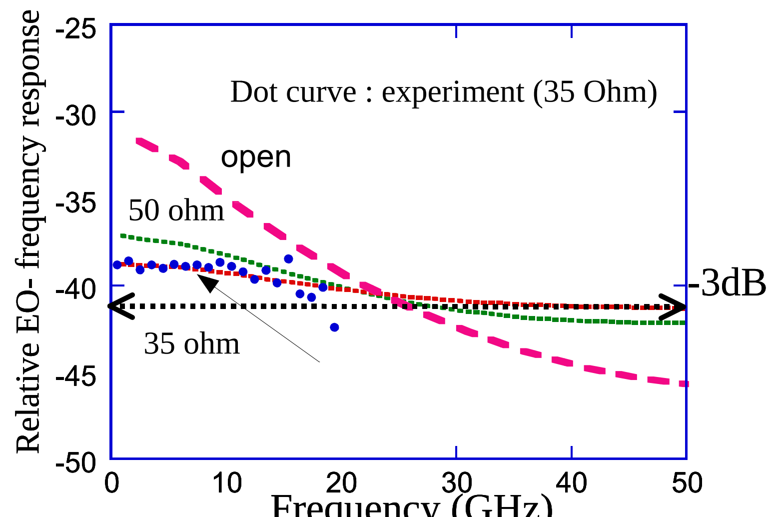
Traveling-wave EAM







J. E. Bowers--funded by RFLICS

Quantum Well Intermixing

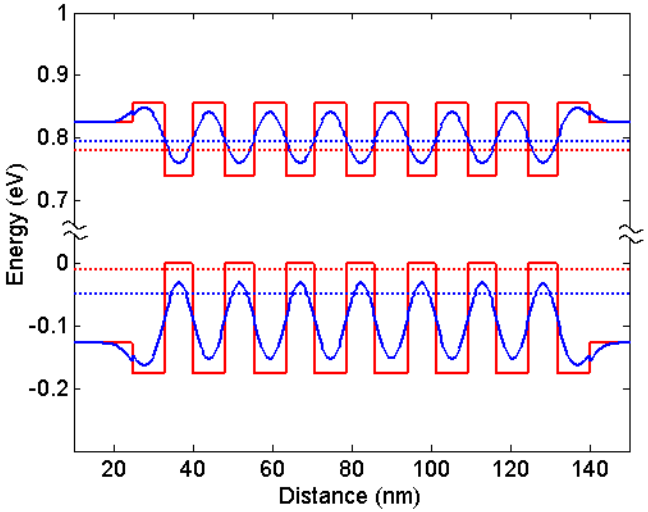
- Impurity-free vacancy-enhanced quantum-well-intermixing

▪ Theory

- Create vacancies
- Thermal process to diffuse vacancies
- Diffusing vacancies allow atoms to exchange positions
- Smears the well/barrier interface, increasing the quantized energy level

▪ Methods

- Ion implantation, sputtering
- Rapid thermal anneal, laser induced



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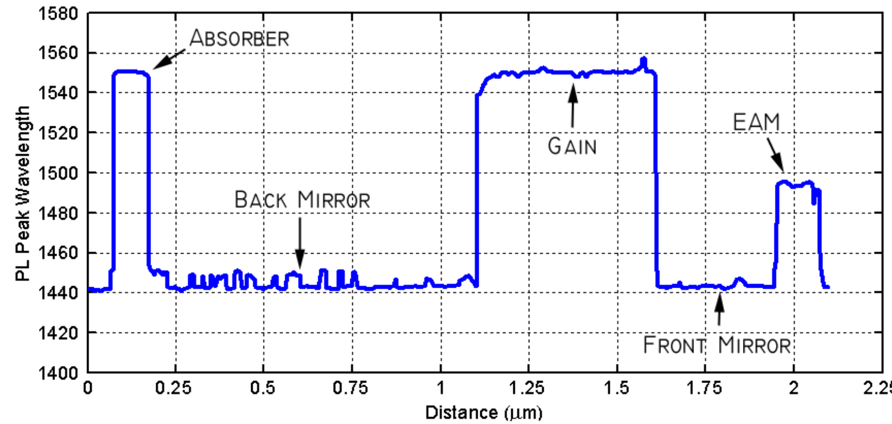
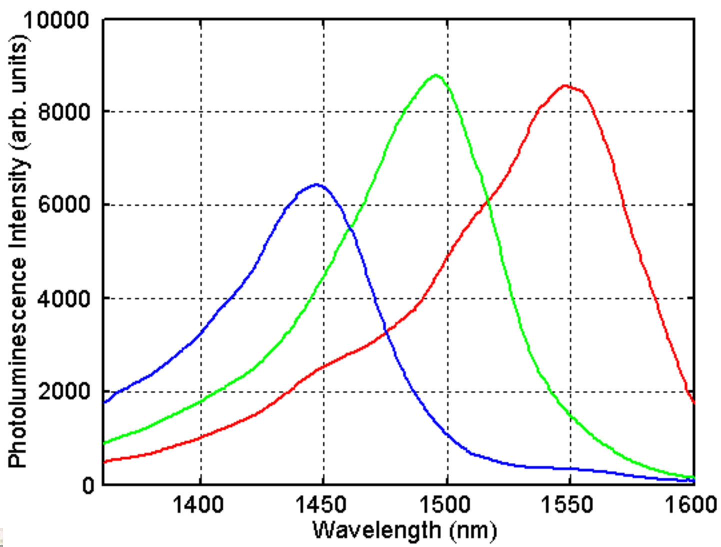
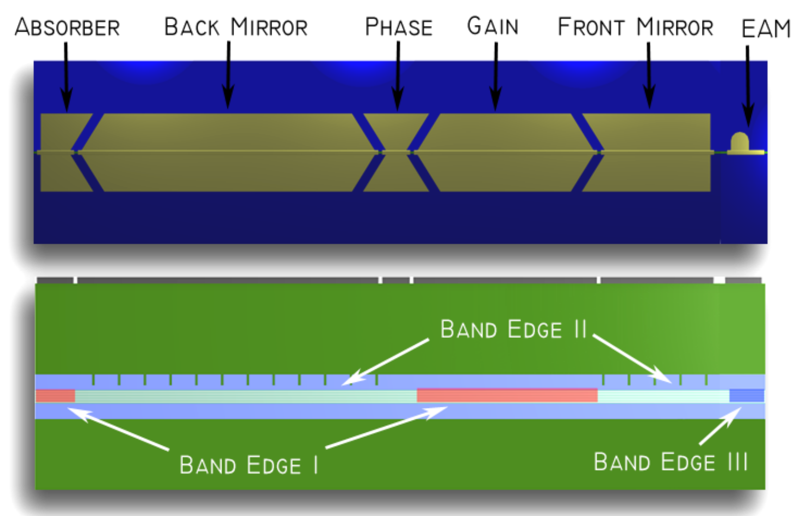
QWI-SGDBR with Integrated EA-Modulator (3 bandgaps)

- Optimized band edges for various devices
- Three band edges across wafer
- Widely-tunable laser/EAM







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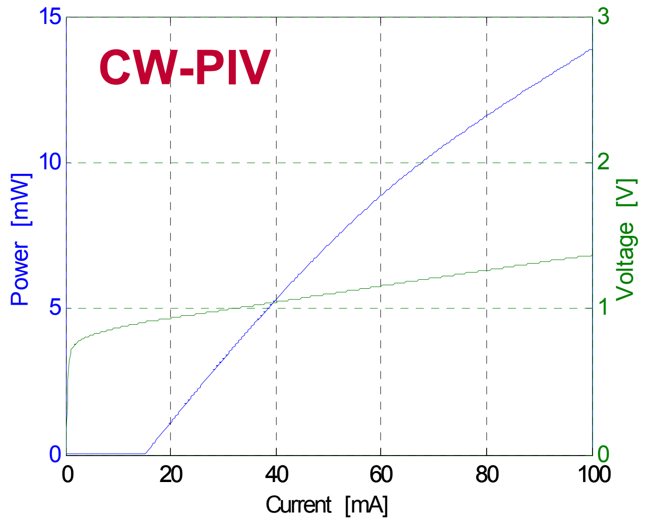
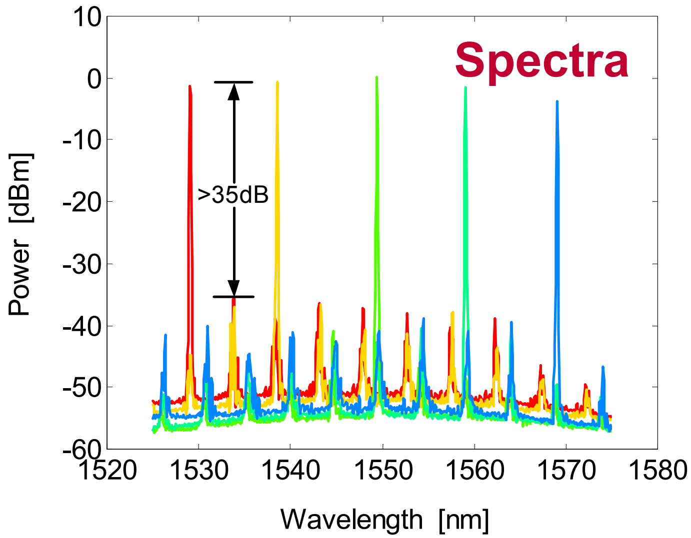
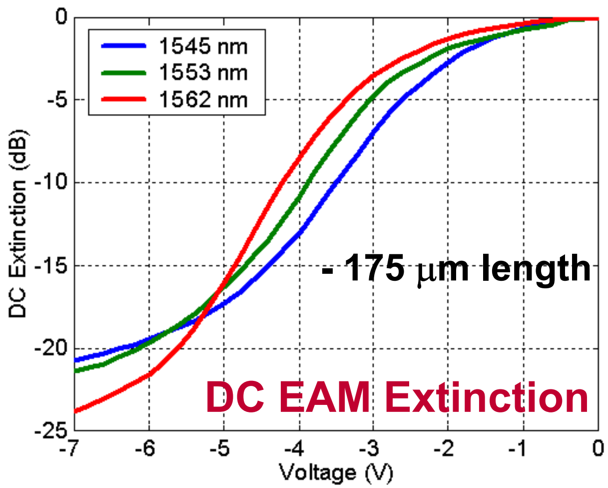
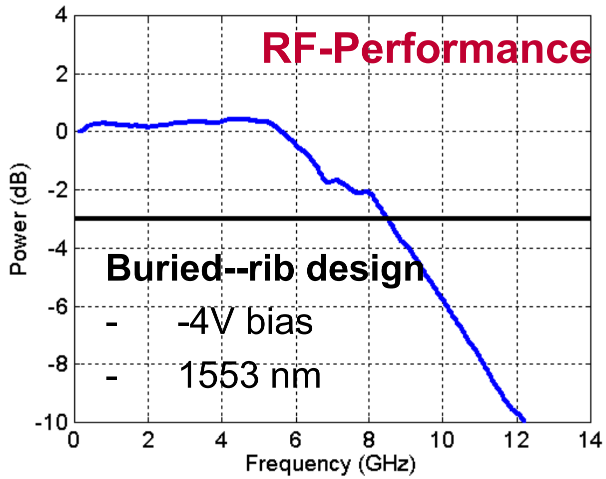
QWI-SGDBR-EAM Transmitter Results









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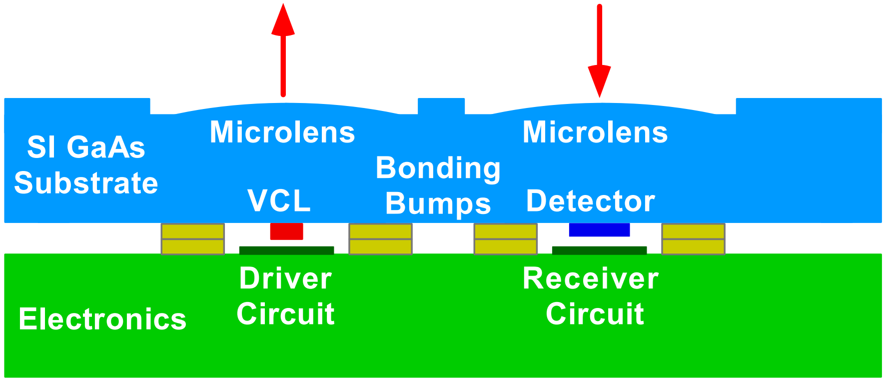
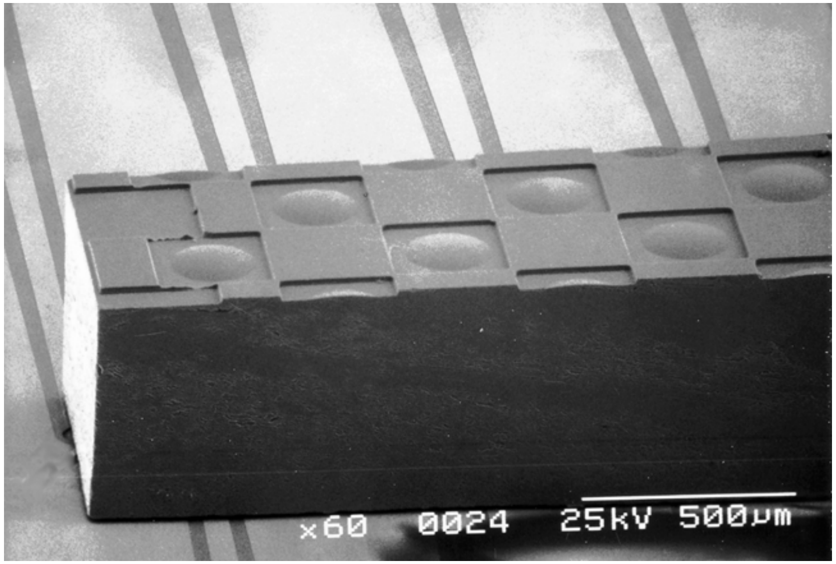
VCSELs for Optical Interconnects

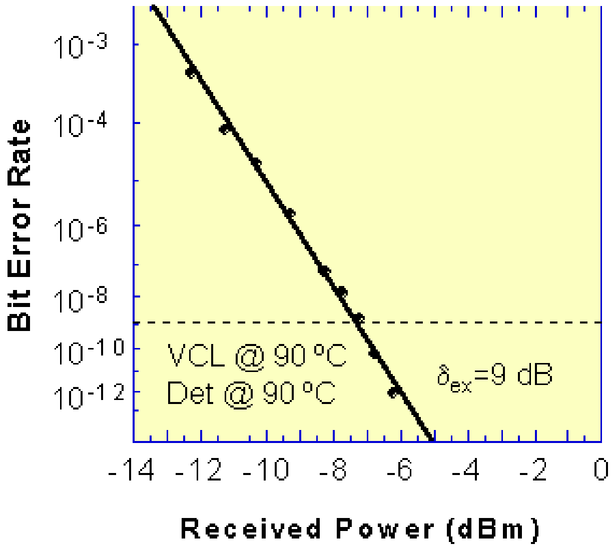




- Prior work has demonstrated state-of-the-art VCSELs and RC-PDs for free-space interconnects

- Microlenses eliminate or relax tolerances on external optics

- Error-free links from 0 – 90C



DARPA FSOI program

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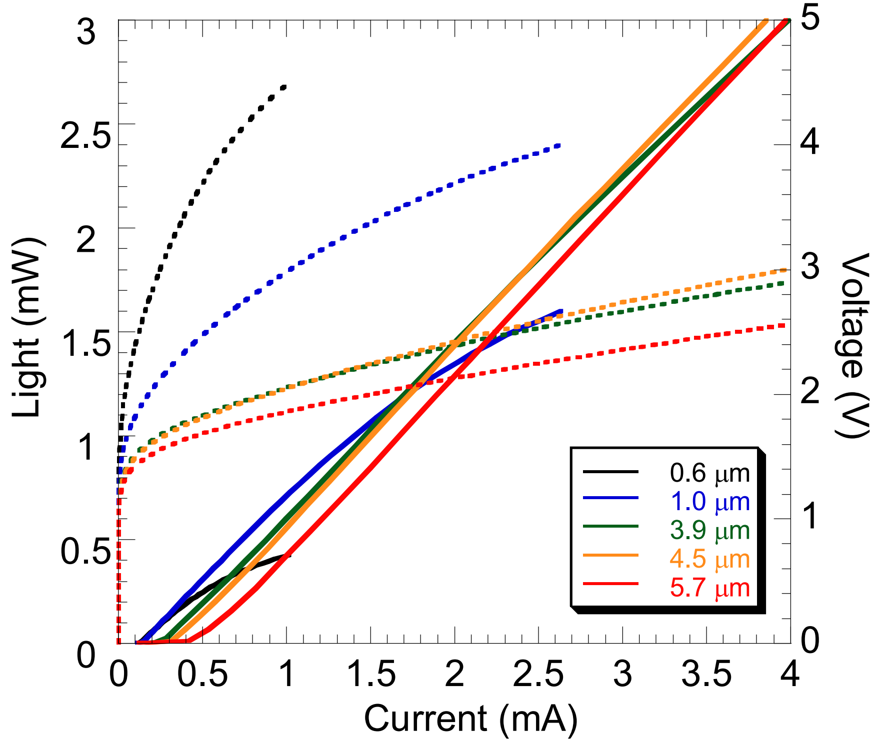
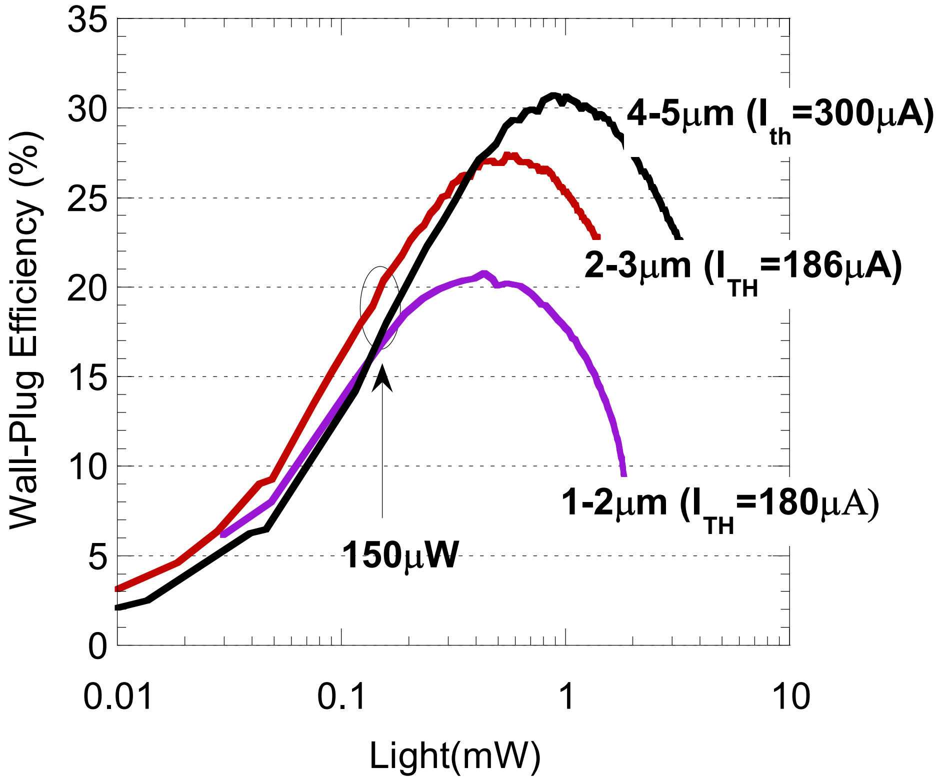
980 nm VCSEL P-I-V & Power efficiency





- Thresholds of 125 µA for 0.6 µm devices
- Optical losses almost eliminated with tapered apertures at the 1st null

- Wall-plug of 30% at 1mW output power

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Progress on C2OI

- **Transmitter:**
  - Waveguide design work nearing completion--initial laser optimization studies initiated
  - QWI for Al-free actives on GaAs initiated--experimental work begun
  - Laser-modulator axial design work initiated—need data for intermixed EAMs

- **Receiver:**
  - Digital receiver architecture investigation begun
  - First generation high-saturation-power PDA photodetector design complete
  - Initial demonstration of concept completed.

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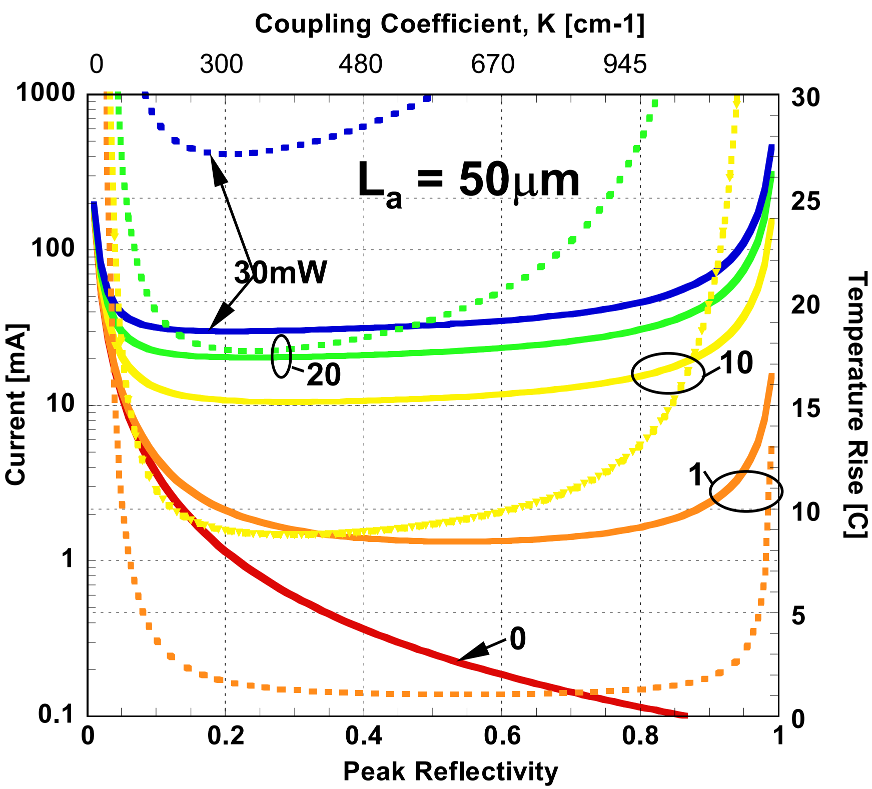
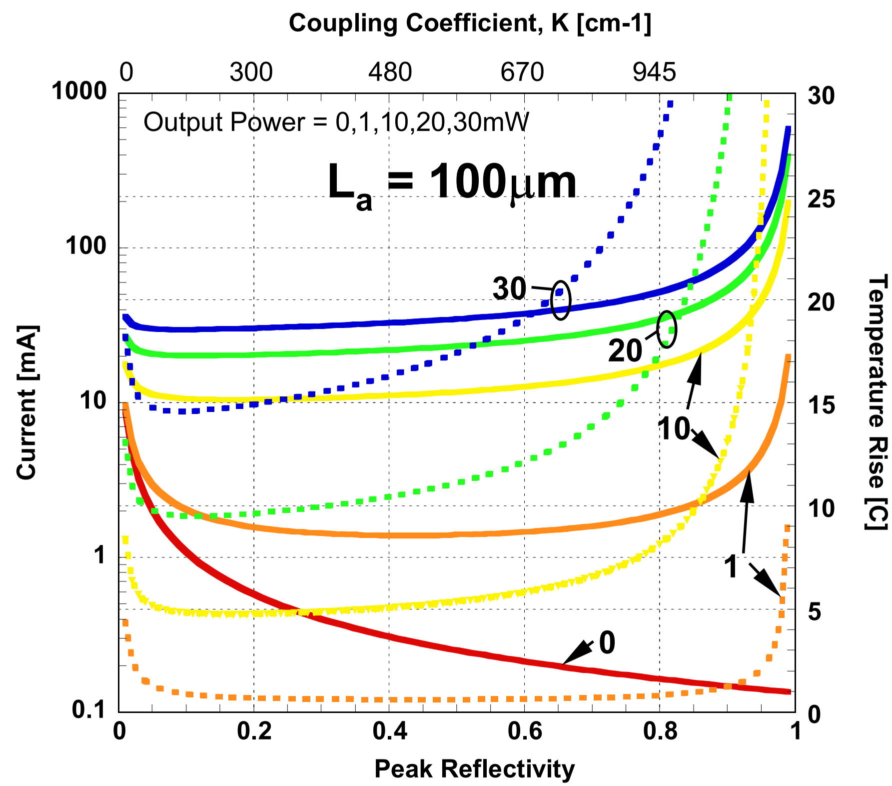
Transmitter Design: Current and Temp rise for Constant Powers

Required current (solid) and Temperature Rise (dotted) vs. Front Mirror Reflectivity for $L_g = 20\mu m$





Design Curves for $W = 2\mu m$, $N_{qw} = 3$, $R_b = 90\%$, $\eta_i = 90\%$, $\alpha_{ia} = \alpha_{im} = 5cm^{-1}$, $\Gamma g_o = 50cm^{-1}$

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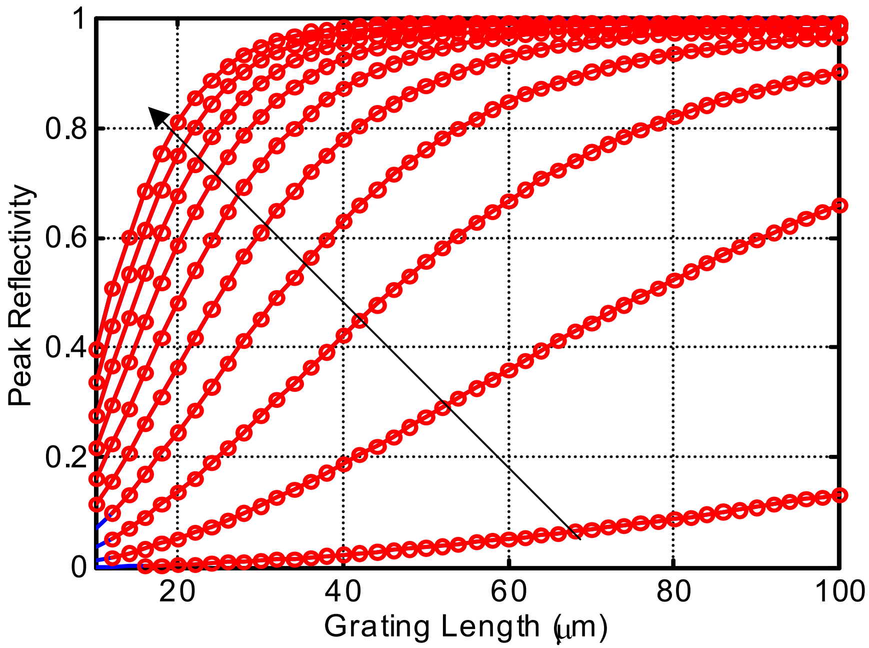
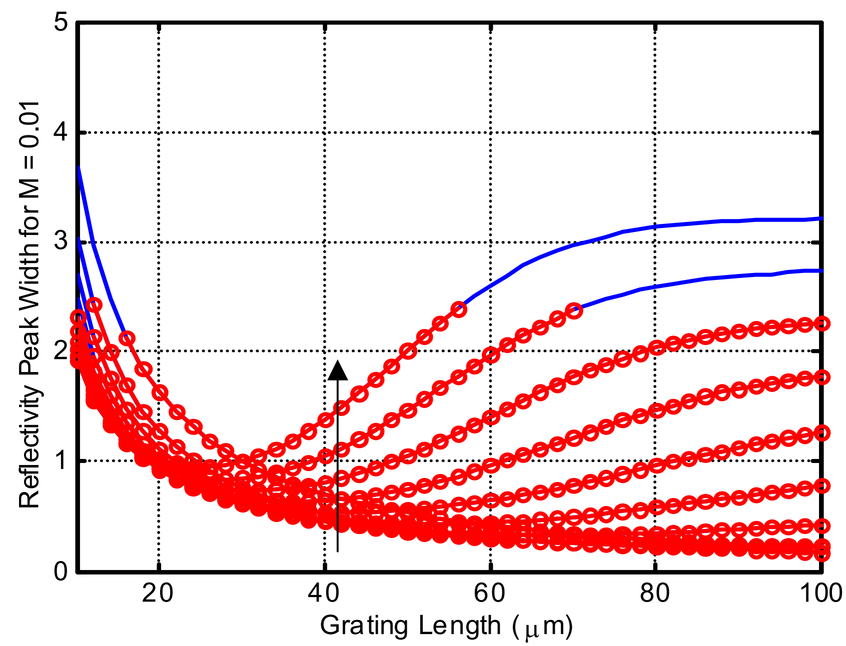
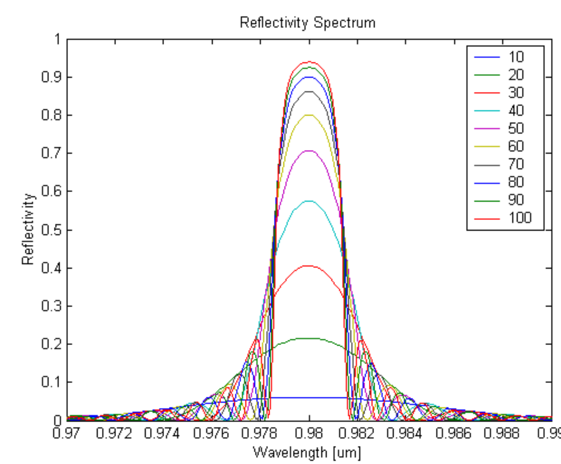
DBR Mirror Design







Red indicates designs for SMSR>=30dB

For increasing kappa 50:100:950 cm^{-1}

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GaAs Lattice-Matched Bandgaps

- Offsets in blue #s to GaAs
- Bandgaps in black
- Units are meV

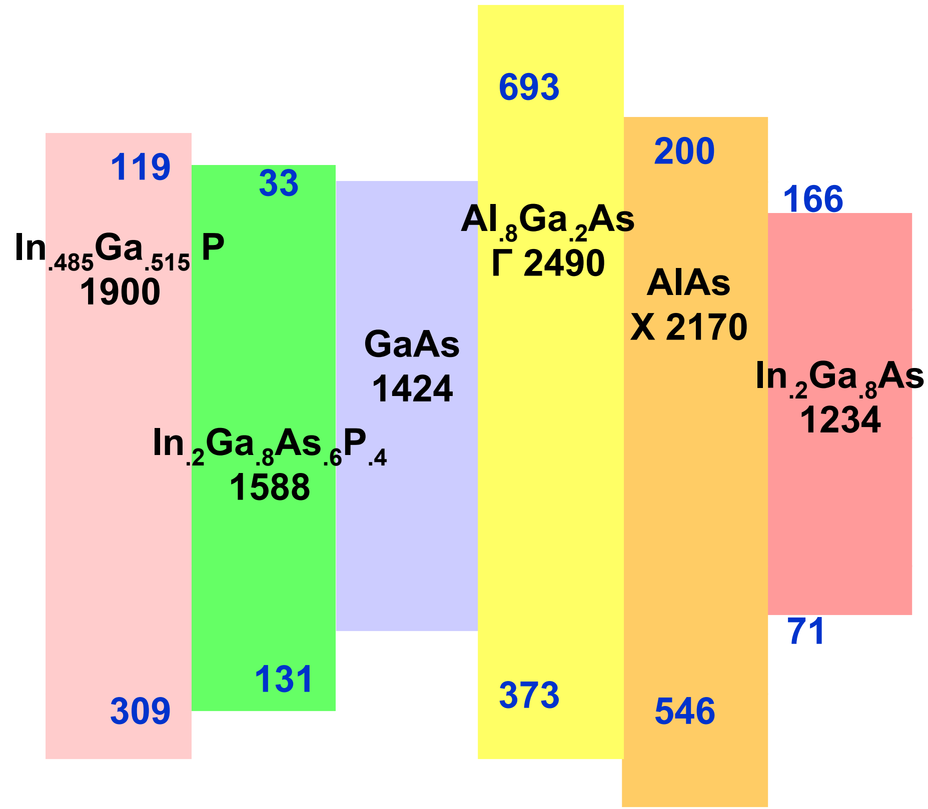
Offsets to GaAs

$In_{.2}Ga_{.8}As\ \Delta E_C = .628\ \Delta E_g$

$In_{.2}Ga_{.8}As_{.6}P_{.4}\ \Delta E_C = .2\ \Delta E_g$

$In_{.485}Ga_{.515}P\ \Delta E_C = .35\ \Delta E_g$

$Al_{.80}Ga_{.20}As\ \Delta E_C = .65\ \Delta E_g$



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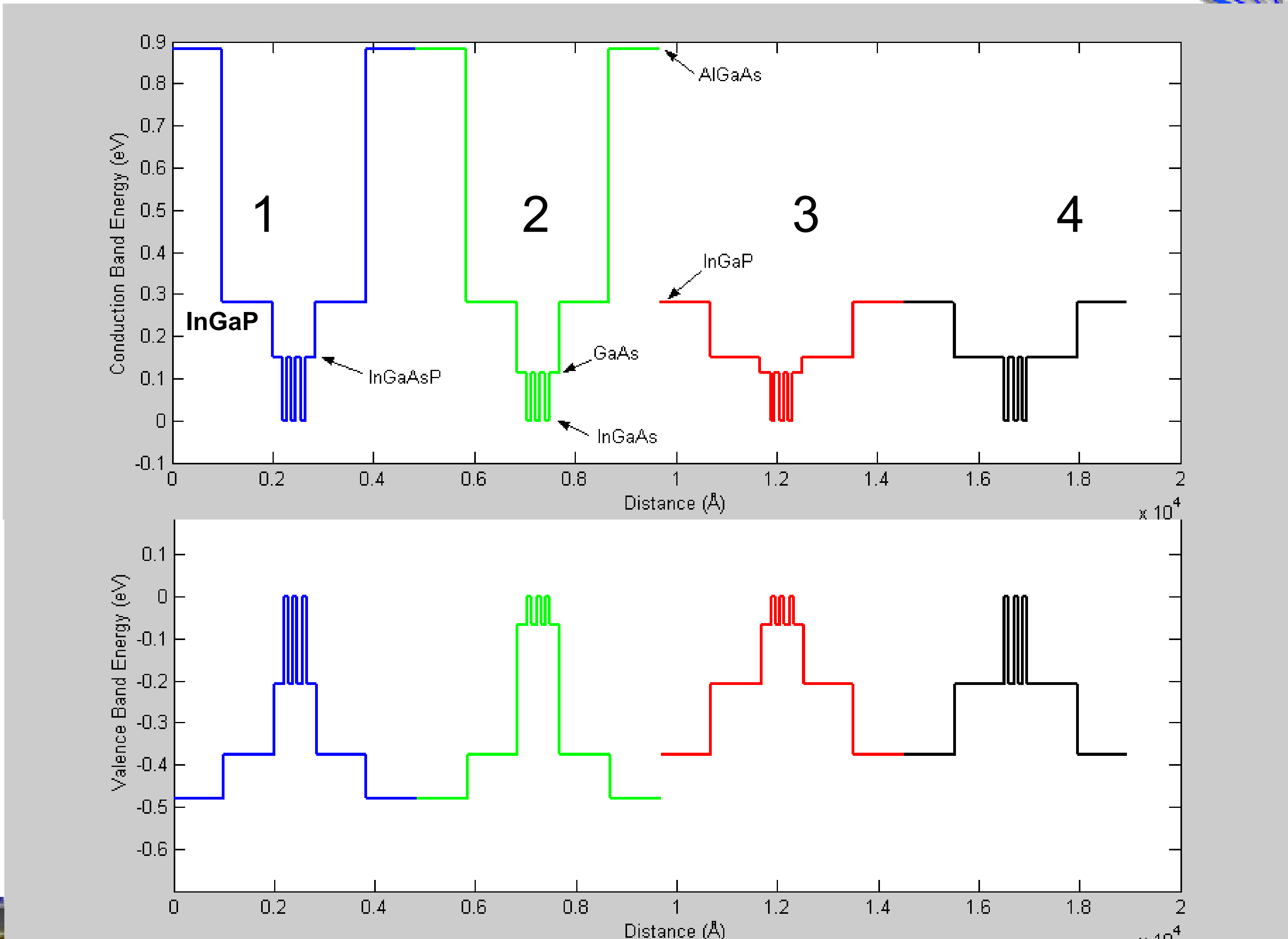
Active Region Designs



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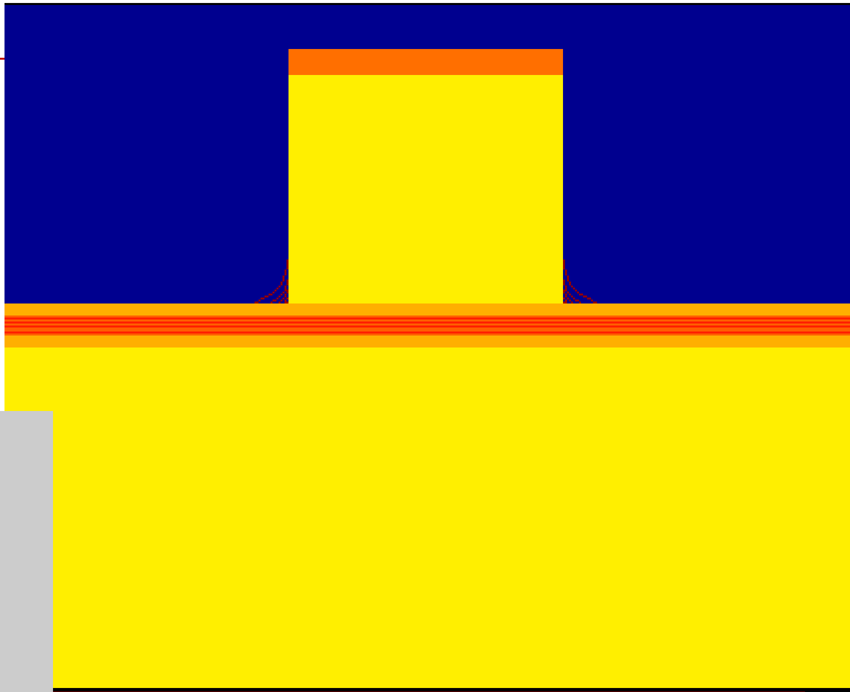
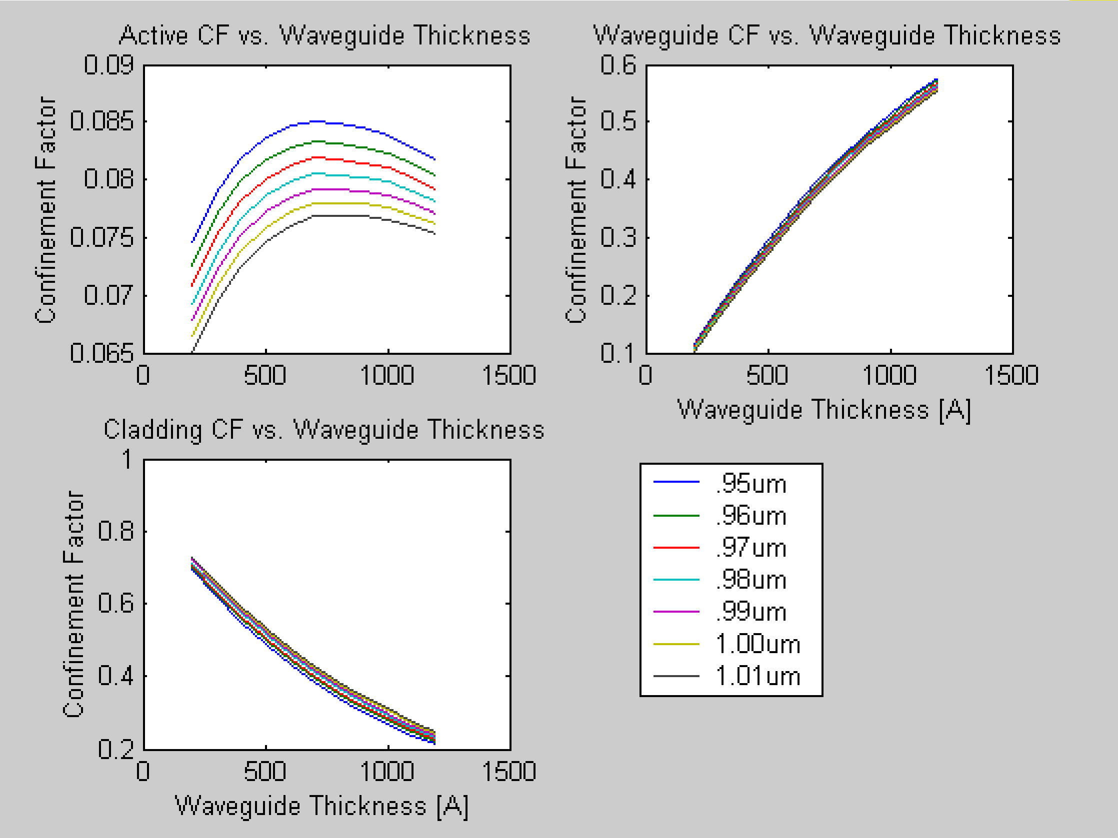
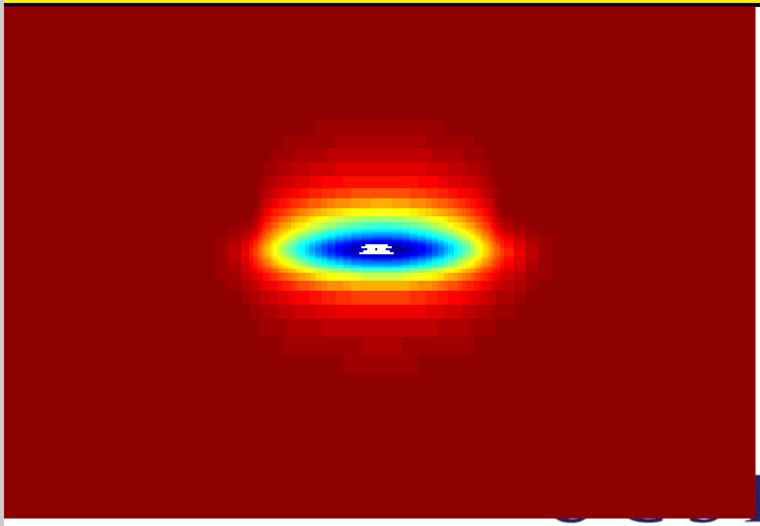
2D Mode Solver Simulations

Optimize Waveguide Thickness

Design #1, 3 QWs, 2.0μm ridge
75Å Wells, 80Å Barriers
Top and Bottom Half of WG = 700Å each







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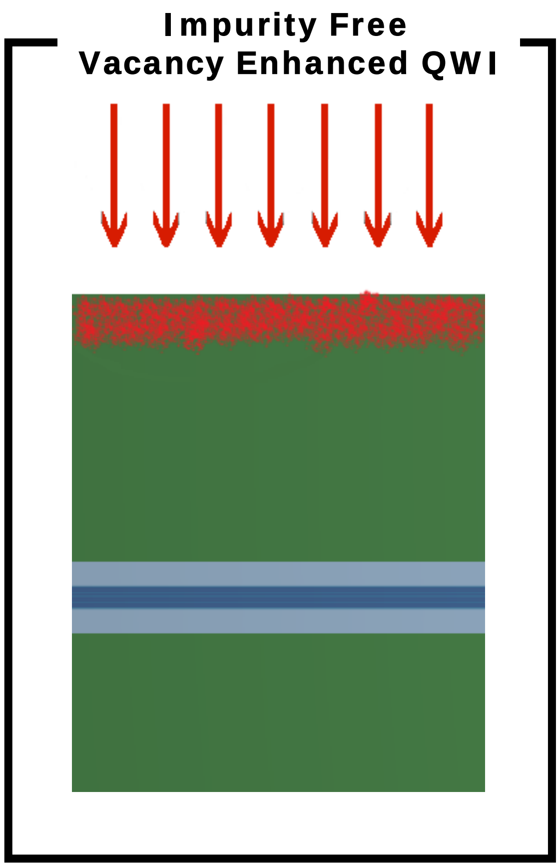
Future QWI Process



P^+ Implant into 4500A InGaP sacrificial layer.

RTA to drive vacancies into Active Region to intermix quantum wells.

Etch off sacrificial layer.

Regrow top cladding.

Milestones

- **Transmitter (UCSB):**
  - Design & simulate small footprint IPSEL-Mod — 6 mo.
  - Demo laser-mod (P_0 > 10 mW; f_c > 15 GHz) — 15 mo.
  - Demo 4-element array module and deliver samples — 18 mo.
  - Demo efficient 40Gb/s IPSEL-Mod array module and deliver samples — 36 mo.

- **Receiver (UT-Austin):**
  - Design & simulate PDA and digital receiver — 6 mo.
  - Demo PDA (P_{sat} > 10 mW; f_c > 40 GHz) — 15 mo.
  - Demo 4-element array module and deliver samples — 18 mo.
  - Demo efficient 40Gb/s digital receiver array module and deliver samples — 36 mo.